



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
-----------------	-------------	----------------------	---------------------	------------------

10/691.085

10/22/2003

Tsuyoshi Ogawa

09792909-5704

9289

26263

7590

07/05/2006

SONNENSCHN NATH & ROSENTHAL LLP

P.O. BOX 061080

WACKER DRIVE STATION, SEARS TOWER

CHICAGO, IL 60606-1080

EXAMINER

WOOD, KEVIN S

ART UNIT

PAPER NUMBER

2874

DATE MAILED: 07/05/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/691,085

Applicant(s)

OGAWA, TSUYOSHI

Examiner

Kevin S. Wood

Art Unit

2874

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE \_\_\_\_ MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 25 April 2006.  
2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.  
3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-8 and 18-20 is/are pending in the application.  
4a) Of the above claim(s) \_\_\_\_ is/are withdrawn from consideration.  
5) ☐ Claim(s) \_\_\_\_ is/are allowed.  
6) ☒ Claim(s) 1-8 and 18-20 is/are rejected.  
7) ☐ Claim(s) \_\_\_\_ is/are objected to.  
8) ☐ Claim(s) \_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.  
10) ☐ The drawing(s) filed on \_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☒ All b) ☐ Some \* c) ☐ None of:  
1. ☒ Certified copies of the priority documents have been received.  
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_.  
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).  
\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☐ Notice of References Cited (PTO-892)  
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)  
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_.

- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_.  
5) ☐ Notice of Informal Patent Application (PTO-152)  
6) ☐ Other: \_\_\_\_.



## **FINAL REJECTION**

### ***Response to Arguments***

1. This action is responsive to the Response filed on 25 April 2006. No claims have been amended. No claims have been added. Claims 1-8 and 18-20 are remain pending in the application. Claims 9-17 and 21-25 have been withdrawn.

2. Applicant's arguments filed 25 April 2006 have been fully considered but they are not persuasive. The examiner has thoroughly reviewed the applicant's arguments but firmly believes the cited references to reasonably and properly meet the claimed limitations. The applicant's primary argument was that U.S. Patent No. 6,892,398 to Ouchi does not disclose all the limitations of the claimed invention of claim 1 or claim 18. Specifically the applicant argues that the Ouchi reference does not discloses the optical interconnect circuit (276,278) being mounted above or below the micro interconnect circuit section (275).

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., the optical element being mounted above or below the micro interconnect circuit section) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

3. Therefore, the examiner respectfully disagrees with the applicant's argument.

The applicant appears to be arguing limitations which have not been claimed. Claims 1 and 18 do not recite the limitation that the optical interconnect circuit must be mounted above or below the micro interconnect circuit section. Instead the claims recite only that both the optical interconnect circuit and the micro interconnect circuit are mounted on the base substrate. The language of the claim does not preclude the micro interconnect circuit (275) and the optical interconnect circuit (276,278) from being mounted within cladding layers (277) while being mounted on a base substrate (273) as shown by the Ouchi reference.

The applicant has failed to point out any *claimed* limitations which the Ouchi reference fails to disclose or make obvious. Therefore, the rejections are believed to be reasonably and fair.

#### ***Claim Rejections - 35 USC § 103***

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 1-8 and 18-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,829,398 to Ouchi.

Referring to claims 1-8, the Ouchi reference discloses an optoelectronic comprising: a base substrate section having an interconnect layer (279) formed on an insulating substrate (273); a micro interconnect circuit section having a micro electrical interconnect layer (275) which is finer than the interconnect layer of the base substrate section, formed on an insulating layer (277); and an optical interconnect circuit section adapted to transfer and/or receive an optical signal and provided with an optical waveguide (276) having an input section and an output section an optical signal at opposite ends thereof; and an optical element composed of a light emitting device (278) with a light emitting section thereof facing the input section and a photo detecting device (278) with a photo detecting section thereof facing the output section; wherein the micro interconnect circuit section and the optical interconnect circuit section are mounted on the base substrate section so as to transmit an electrical signal and an optical signal. See Fig. 18 along with its respective portion of the specification. It should be noted that this claim is a device claim, therefore the limitations directed to how each component were made are not considered during the determination of patentability of the device. The Ouchi reference does not appear to specifically disclose that the insulating layer is a resin layer. Resin layers are known in the art and the application does not disclose the criticality or unexpected results from using a resin to form the insulating layer. It would have been obvious to one having ordinary skill in the art at the time the invention was made to utilize a resin for the insulating layer, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended. *In re Leshin*, 125 USPQ 416.

Referring to claims 18-20, the Ouchi reference discloses an optoelectronic comprising: a base substrate section having an interconnect layer (279) formed on an insulating substrate (273); a micro interconnect circuit section having a micro electrical interconnect layer (275) which is finer than the interconnect layer of the base substrate section, formed on an insulating layer (277); and an optical interconnect circuit section adapted to transfer and/or receive an optical signal and provided with an optical waveguide (276) having an input section and an output section an optical signal at opposite ends thereof; and an optical element composed of a light emitting device (278) with a light emitting section thereof facing the input section and a photo detecting device (278) with a photo detecting section thereof facing the output section; wherein the micro interconnect circuit section and the optical interconnect circuit section are mounted on the base substrate section so as to transmit an electrical signal and an optical signal. The Ouchi reference also discloses electronic components (270) mounted on a surface of the base substrate (273), and electrically connected to one of the interconnect layers (275,279) and the optical elements (278). See Fig. 18 along with its respective portion of the specification. It should be noted that this claim is a device claim, therefore the limitations directed to how each component were made are not considered during the determination of patentability of the device. The Ouchi reference does not appear to specifically disclose that the insulating layer is a resin layer. Resin layers are known in the art and the application does not disclose the criticality or unexpected results from using a resin to form the insulating layer. It would have been obvious to one having ordinary skill in the art at the time the invention was made to utilize a resin for the

Art Unit: 2874

insulating layer, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended. *In re Leshin*, 125 USPQ 416.

### ***Conclusion***

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin S. Wood whose telephone number is (571) 272-2364. The examiner can normally be reached on Monday-Thursday (7am - 5:30 pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rodney B. Bovernick can be reached on (571) 272-2344. The fax phone

Art Unit: 2874

number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



Kevin S. Wood  
Patent Examiner